REMARKS

Claims 1 to 22 are pending.

Claims 1, 2, 4 and 5 have been rejected under 35 U.S.C. 102(e) as being anticipated by Hassoun (U.S. Patent No. 6,487,648).

Amended claim 1 recites a digital frequency synthesizer having a variable oscillator, coupled to the delay lock loop.

The Examiner asserts, that as shown in Figure 4, Hassoun discloses a digital clock manager … comprising: a delay lock loop (DLL) (304B) … and a digital frequency synthesizer (304A), coupled to the delay lock loop". The Examiner argues that based on the broadest reasonable interpretation of the claim language a delay lock loop (DLL) can be a digital frequency synthesizer (DFS).

Hassoun in Fig. 5 and col. 5, lines 14-65, describes a DLL as a variable delay line and does not disclose nor suggest the DLL having a variable oscillator. Hence Hassoun does not anticipate claim 1 and claim 1 should now be allowable.

In addition, Applicants assert there may be confusion between a phase-locked loop (PLL) which can be used in an "Integer-N frequency synthesizer" and a DLL, which has mainly a delay function.

A DLL includes a variable delay line and control logic. One example of a DLL works by inserting delay between an input signal and a feedback signal until the two rising edges align, putting the two signals 360° out of phase (meaning they are in phase). While designed for the same basic function, the PLL uses a different architecture to accomplish the task. The main difference between the PLL and DLL is that instead of a delay line, the PLL uses a voltage controlled oscillator (VCO) which generates a feedback signal that approximates the input signal. The PLL control logic compares the input signal to the feedback signal and adjusts the oscillator signal until the rising edge of the input signal aligns with the feedback signal. Because

the feedback loop on a PLL has a divide by N frequency divider circuit, the PLL can be an integer-N frequency synthesizer.

An example of a DLL is shown in Figs. 6 and page 14, line 9 to page 17, line 29 of the specification. An input clock (REF_CLK 602) is delayed via delay line 610 and then phase shifted (further time delayed) via clock phase shifter 650 to produce a delayed input clock signal (O-CLK 604). The DLL, as shown in Fig. 6, tries to align the O_CLK with the skewed clock S_CLK.

A digital frequency synthesizer multiplies and/or divides the input signal frequency. An example of a DFS is described in Fig. 14(a) and page 26, line 13 to page 28, line 10 of the specification.

Thus, Hassoun fails to teach or suggest a digital frequency synthesizer having a variable oscillator as recited by Claim 1. For this reason, Claim 1 is not anticipated by Hassoun. Claims 2, 4 and 5, which depend from Claim 1, are not anticipated by Hassoun for at least the same reasons as Claim 1.

Claims 3, and 6-18 have been objected to as being dependent upon a rejected base claim. The Examiner has indicated that these claims would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. However, because Applicants believe that the base claims are allowable (for reasons stated above), Applicants are not amending Claims 3 and 6-18 at this time.

Applicants note with appreciation the allowance of Claims 19-22.

CONCLUSION

Claims 1-22 are pending in the present application. Reconsideration of Claims 1, 2, 4 and 5 is requested.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 23, 2004..

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